What we claim is:

1. A clock recovery circuit provided to a receiving device which receives digital broadcasts using a VSB modulation method, comprising:

a first band pass filter which, when a symbol rate of a received signal is fs, extracts a signal of an fs/2 frequency component from an in-phase component of a VSB signal which has been converted to baseband;

a second band pass filter which extracts a signal of an fs/2 frequency component from a quadrature-phase component of said VSB signal;

a delay element which delays an output signal of said second band pass filter by Π/4;

a first multiplier which squares an output signal of said first band pass filter;

a second multiplier which squares an output signal of said delay element;

an adder which adds together an output signal of said first multiplier and an output signal of said second multiplier;

a third band pass filter which extracts a signal of an fs frequency component from an output signal of said adder, and outputs a symbol clock received signal;

a phase error detector which detects a phase error between a symbol clock received signal of said third band pass filter and a reference clock of receiving device; and

a loop filter which smoothes a phase error signal which is outputted by said phase error detector.

2. A clock recovery circuit provided to a receiving device which receives digital broadcasts using a VSB modulation method, comprising:

a first band pass filter which, when a symbol rate of a received signal is fs, extracts a signal of an fs/2 frequency component from an in-phase component of a VSB signal which has been converted to baseband;

a second band pass filter which extracts a signal of an fs/2 frequency component from a quadrature-phase component of said VSB signal;

a first low pass filter which extracts a pilot signal from said in-phase component of said VSB signal which has been converted to baseband;

a second low pass filter which extracts a pilot signal from said quadrature-phase component of said VSB signal which has been converted to baseband;

a first complex number arithmetical unit which, when output

signals of said first and said second band pass filters are considered as a first complex number signal, and output signals of said first and said low pass filters are considered as a second complex number signal, divides said first complex number signal by said second complex number signal according to the rules for complex number division;

a third band pass filter which extracts a signal of an fs/2 frequency component from an in-phase component of an output signal of said first complex number arithmetical unit;

a fourth band pass filter which extracts a signal of an fs/2 frequency component from a quadrature-phase component of the output signal of said first complex number arithmetical unit;

a second complex number arithmetical unit which, when output signals of said third and said fourth band pass filters are considered as a third complex number signal, squares said third complex number signal;

a first filter which extracts an in-phase component signal which has frequency fs from an output signal of said second complex number arithmetical unit;

a second filter which extracts a quadrature-phase component signal which has frequency fs from the output signal of said second complex number arithmetical unit;

a phase error detector which, when the output signals of

said first and said second filters are considered as a fourth complex number signal, detects a phase error between a symbol clock received signal included in said fourth complex number signal and a reference clock of receiving device; and

a loop filter which smoothes a phase error signal which is outputted by said phase error detector.

3. A clock recovery circuit according to claim 2, wherein said first and said second filters are high pass filters which pass an fs component when an operating speed of said clock recovery circuit is 2fs, and are band pass filters when the operating speed of said clock recovery circuit is greater than 2fs.

4. A clock recovery circuit provided to a receiving device which receives digital broadcasts using a VSB modulation method, comprising:

a first band pass filter which, when a symbol rate of a received signal is fs, extracts a signal of an fs/2 frequency component from an in-phase component of a VSB signal which has been converted to baseband;

a second band pass filter which extracts a signal of an fs/2 frequency component from a quadrature-phase component of said VSB

signal;

a first low pass filter which extracts a pilot signal from said in-phase component of said VSB signal which has been converted to baseband;

a second low pass filter which extracts a pilot signal from said quadrature-phase component of said VSB signal which has been converted to baseband;

a first complex number arithmetical unit which, when the output signals of said first and said second band pass filters are considered as a first complex number signal, and output signals of said first and said low pass filters are considered as a second complex number signal, divides said first complex number signal by said second complex number signal according to rules for complex number division;

a third band pass filter which extracts a signal of the fs/2 frequency component from an in-phase component of an output signal of said first complex number arithmetical unit;

a fourth band pass filter which extracts a signal of the fs/2 frequency component from a quadrature-phase component of said output signal of said first complex number arithmetical unit;

a reference clock of receiving device generator which, with a reference clock of receiving device frequency on a complex

number plane being taken as fs', outputs a reference clock of receiving device having a frequency of fs'/2 as a fourth complex number signal;

a second complex number arithmetical unit which, when output signals of said third and said fourth band pass filters are considered as a third complex number signal, divides said third complex number signal by said fourth complex number signal according to said rules for complex number division;

a third low pass filter which extracts only an in-phase component which has frequency (fs-fs')/2 from an output signal of said second complex number arithmetical unit;

a fourth low pass filter which extracts only a quadrature-phase component which has frequency (fs-fs')/2 from the output signal of said second complex number arithmetical unit;

a phase error detector which, when an output signals of said third and fourth low pass filters are considered as a fifth complex number signal, outputs a frequency of said fifth complex number signal as a frequency error of the symbol clock, and outputs a phase of said fifth complex number signal as a phase error of the symbol clock; and

a loop filter which smoothes a phase error signal which is outputted by said phase error detector.

5. A clock recovery circuit according to claim 4, wherein, in a complex number plane defined by an I-axis and a Q-axis, said reference clock signal generator outputs in order (I, Q) signals whose phase differs by a phase difference of $\pi/4$ at a clock signal frequency of 2fs'.

6. A clock recovery circuit provided to a receiving device which receives digital broadcasts using a VSB modulation method, comprising:

a tendency detection section which, when successive symbol data in time series in a VSB signal which has been converted to baseband are termed D1, D2, and D3, detects the tendency from D1 to D3 by the value of symbol data amount of change;

a symbol data error detection section which detects an amount of deviation of a D2 symbol value with respect to the proper symbol data (the proper mapping value);

a multiplier which multiplies together an output value of said tendency detection section and an output value of said symbol value error detection section;

a region decision section which, based upon a symbol value of D2, decides whether a currently received symbol is present in a data update region or is present in a data holding region, and which performs control so as, if said currently received symbol

is present in said data update region, to output a result of multiplication by said multiplier, while, if said currently received symbol is present in said data holding region, not to output said result of multiplication by said multiplier;

an averaging circuit which averages the output signal of said region decision section once every predetermined number of times; and

a loop filter which smoothes a phase error signal which is outputted by said averaging circuit.

7. A clock recovery circuit according to claim 6, wherein said tendency detection section subtracts D3 from D1, and detects said tendency by whether a resulting value is positive or negative.

8. A clock recovery circuit according to claim 6, wherein said symbol value error detection section detects a symbol value error by subtracting a proper mapping value from D2.

9. A clock recovery circuit according to claim 6, wherein said region decision section performs region decision based upon a "Stop and Go" algorithm.